WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cell blocks, wherein each of the memory cell blocks includes a plurality of memory cells and a plurality of word lines connected to the memory cells;

a plurality of row decoders connected to the plurality of memory cell blocks, wherein each of the row decoders selects one of the word lines in an associated one of the memory cell blocks;

a plurality of sense amp groups connected to the plurality of row decoders, wherein each of the sense amp groups amplifies cell information read from the plurality of memory cells of an associated one of the memory cell blocks;

a plurality of block control circuits connected to the plurality of memory cell blocks, wherein each of the block control circuits simultaneously selects multiple word lines in an associated one of the memory cell blocks and generates a sense amp control signal; and

a plurality of sense amp drive circuits connected to the plurality of block control circuits and the plurality of sense amp groups, wherein each of the sense amp drive circuits selectively activates an associated one of the sense amp groups based on the sense amp control signal of the associated one of the block control circuits;

wherein each of the block control circuits generates at least one reset signal and provides the reset signal to an associated one of the row decoders and to an associated one of the sense amp drive circuits, the reset signal being provided to the associated one of the row decoders so that the timing for selecting the word lines with the row decoders differs between each block, and the reset signal being provided to the associated one of the sense amp drive

circuits so that inactivation of the plurality of sense amp groups differs between each block.

2. The device according to claim 1, wherein each of the block control circuits generates the reset signal based on a block address signal that selects one of the plurality of memory cell blocks.

3. The device according to claim 2, wherein each of the block control circuits includes:

a block selection circuit for generating a block selection signal based on the block address signal;

a word line set signal generation circuit connected to the block selection circuit for generating a word line set signal to select one of the word lines; and

a word line reset signal generation circuit connected to the block selection circuit for generating the word line reset signal to stop selecting the word line based on the block selection signal;

wherein the word line reset signal generation circuit generates the word line reset signal based on the block address signal, which is provided after the block selection signal is output.

4. The device according to claim 3, wherein each of the sense amp drive circuits inactivates the associated sense amps based on the word line reset signal.

5. The device according to claim 2, wherein each of the block selection circuits resets the block selection signal based on the block address signal, which is provided after the block selection signal is output.

6. The device according to claim 3, further comprising:

a timing signal generation circuit connected to the plurality of sense amp drive circuits for generating a sense amp set timing signal to control activation of the plurality of sense amps;

wherein each of the sense amp drive circuits activates the associated sense amps based on the block selection signal and the sense amp set timing signal after a predetermined time elapses from when the first word line is selected.

7. The device according to claim 6, wherein each of the sense amp drive circuits includes a latch circuit.

8. A method for conducting a multiple word line selection test on a semiconductor memory device provided with a plurality of memory cell blocks, which include a first memory cell block and a second memory cell block, each of the memory cell blocks having a plurality of memory cells and a plurality of word lines connected to the memory cells, and a plurality of sense amp groups connected to the first and second memory cell blocks, each of the sense amp groups amplifying cell information read from the plurality of memory cells of an associated one of the memory cell blocks, the method comprising:

a first step for activating one of the plurality of word lines in the first memory cell block and activating the sense amp group associated with the first memory cell block after a predetermined time;

a second step for activating word lines other than the one that has been activated in the first memory cell block;

a third step for activating one of the plurality of

word lines in the second memory cell block and activating the sense amp group associated with the second memory cell block after a predetermined time; and

a fourth step for activating word lines other than the one that has been activated in the second memory cell block;

wherein the third and fourth steps are performed while the first and second steps are continuously performed or the second and fourth steps are performed while the first and third steps are continuously performed.

9. A method for conducting a multiple word line selection test on a semiconductor memory device provided with a plurality of memory cell blocks, which include a first memory cell block and a second memory cell block, each of the memory cell blocks having a plurality of memory cells and a plurality of word lines connected to the memory cells, and a plurality of sense amp groups connected to the first and second memory cell blocks, each of the sense amp groups amplifying cell information read from the plurality of memory cells of an associated one of the memory cell blocks, the method comprising:

a first step for inactivating multiple word lines in the first memory cell block and the sense amp group associated with the first memory cell block; and

a second step for inactivating multiple word lines in the second memory cell block and the sense amp group associated with the second memory cell block after performing the first step.

10. A method for conducting a multiple word line selection test on a semiconductor memory device provided with a plurality of memory cell blocks, which include a first memory cell lock and a second memory cell block, each

of the memory cell blocks having a plurality of memory cells and a plurality of word lines connected to the memory cells, and a plurality of sense amp groups connected to the first and second memory cell blocks, each of the sense amp groups amplifying cell information read from the plurality of memory cells of an associated one of the memory cell blocks, the method comprising:

a first step for activating one of the plurality of word lines in the first memory cell block and activating the sense amp group associated with the first memory cell block after a predetermined time;

a second step for activating word lines other than the one that has been activated in the first memory cell block;

a third step for activating one of the plurality of word lines in the second memory cell block and activating the sense amp group associated with the second memory cell block after a predetermined time;

a fourth step for activating word lines other than the one that has been activated in the second memory cell block;

a fifth step for inactivating multiple word lines in the first memory cell block and the sense amp group associated with the first memory cell block; and

a sixth step for inactivating multiple word lines in the second memory block and the sense amp group associated with the second memory block after performing the fifth step;

wherein the third and fourth steps are performed while the first and second steps are continuously performed or the second and fourth steps are performed while the first and third steps are continuously performed.

11. A semiconductor memory device comprising:

a plurality of memory cell blocks, wherein each of the

memory cell blocks includes a plurality of memory cells and a plurality of word lines connected to the memory cells;

a plurality of row decoders connected to the plurality of memory cell blocks, wherein each of the row decoders selects one of the word lines in an associated one of the memory cell blocks;

a plurality of sense amp groups connected to the plurality of memory cell blocks, wherein each of the sense amp groups amplifies cell information read from the plurality of memory cells of an associated one of the memory cell blocks;

a plurality of block control circuits connected to the plurality of row decoders, wherein each of the block control circuits simultaneously selects multiple word lines in an associated one of the memory cell blocks and generates a sense amp control signal; and

a plurality of sense amp drive circuits connected to the plurality of block control circuits and the plurality of sense amp groups, wherein each of the sense amp drive circuits selectively activates an associated one of the sense amp groups based on the sense amp control signal of the associated one of the block control circuits, each of the sense amp drive circuits including a latch circuit.

12. The device according to claim 11, further comprising:

a timing signal generation circuit connected to the plurality of sense amp drive circuits for generating a sense amp set timing signal, which selectively controls activation of the plurality of sense amp groups, and a sense amp reset timing signal;

wherein the latch circuit receives the sense amp set timing signal and the sense amp reset timing signal.

13. The device according to claim 11, wherein the block control circuit includes a word line reset signal generation circuit for generating a word line reset signal that stops selecting the plurality of word lines, wherein the latch circuit receives the word line reset signal including block information.